CHAPTER: 3

PROGRAMMABLE PERIPHERAL INTERFACE & ELECTROMECHANICAL DEVICES INTERFACING
Introduction to 8255 PPI

- The Intel 8255A is a high-performance, general purpose programmable I/O device
  - is designed for use with all Intel and most other microprocessors

- The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to a microprocessor.

- It provides 24 I/O pins
  - Can be individually programmed in 2 groups of 12
  - Used in 3 major modes of operation
  - Each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs
Introduction to 8255 PPI

- The 8255 is a widely used, programmable parallel I/O device.
- It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O.
- It is flexible, versatile and economical (when multiple I/O ports are required).
- It is an important general purpose I/O device that can be used with almost any microprocessor.
Control Logic of 8255

- **RD (Read)**: is signal enables the Read operation. When the signal is low, microprocessor reads data from a selected I/O port of 8255.

- **WR (Write)**: This is an input line driven by the microprocessor. A low on this line indicates write operation.

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- **CS**: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
Control Logic of 8255

PA<sub>7</sub>-PA<sub>0</sub>: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.

PC<sub>7</sub>-PC<sub>4</sub>: Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.

PC<sub>3</sub>-PC<sub>0</sub>: These are the lower port C lines, other details are the same as PC<sub>7</sub>-PC<sub>4</sub> lines.

PB<sub>0</sub>-PB<sub>7</sub>: These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

D<sub>0</sub>-D<sub>7</sub>: These are the data bus lines those carry data or control word to/from the microprocessor.

RESET: A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.
8255A BLOCK DIAGRAM AND FUNCTIONAL DESCRIPTION

- It has a 40 pins of 4 groups.
  1. Data bus buffer
  2. Read Write control logic
  3. Group A and Group B controls
  4. Port A, B and C
8255A BLOCK DIAGRAM AND FUNCTIONAL DESCRIPTION
Contd…

- **Data Bus Buffer**
  - This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus.
  - Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.
  - Control words and status information are also transferred through the data bus buffer.

- **Read/Write and Control Logic**
  - Manage all of the internal and external transfers of both Data and Control or Status words.
  - It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.
  - This unit accepts control signals (RD, WR) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
Group A and Group B Controls

These block receive control from the CPU and issues commands to their respective ports.

The control word contains information such as “mode”, “bit set”, “bit reset”, etc

- Each of the Control blocks (Group A and Group B)
  - accepts ``commands'' from the Read/Write Control Logic,
  - receives ``control words'' from the internal data bus
  - issues the proper commands to its associated ports

- Control Group A - Port A and Port C upper (C7-C4)
- Control Group B - Port B and Port C lower (C3-C0)
Ports A, B, and C

- The 8255A contains three 8-bit ports (A, B, and C)
- All can be configured in a wide variety of functional characteristics
- Each has its own special features or “personality” to further enhances the power and flexibility of the 8255A
  - **Port A**: One 8-bit data output latch/buffer and one 8-bit input latch buffer
  - **Port B**: One 8-bit data input/output latch/buffer
  - **Port C**: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)
    - This port can be divided into two 4-bit ports under the mode control
Control register controls the overall operation of 8255

All three ports A, B and C are grouped into two
These are two basic modes of operation of 8255.

- **I/O mode** and
- **Bit Set-Reset mode (BSR).**

In **I/O mode**, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.

Under the **I/O mode** of operation, further there are three modes of operation of 8255, so as to support different types of applications,

- **mode 0,**
- **mode 1** and
- **mode 2.**
<table>
<thead>
<tr>
<th>CS</th>
<th>A₁</th>
<th>A₀</th>
<th>Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Port A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port B</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Port C</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Control Register</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
<td>x</td>
<td>8255 is not selected</td>
</tr>
</tbody>
</table>
### Contd.

<table>
<thead>
<tr>
<th>RD</th>
<th>WR</th>
<th>CS</th>
<th>A&lt;sub&gt;1&lt;/sub&gt;</th>
<th>A&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Input (Read) cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Port A to Data bus</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port B to Data bus</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Port C to Data bus</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CWR to Data bus</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RD</th>
<th>WR</th>
<th>CS</th>
<th>A&lt;sub&gt;1&lt;/sub&gt;</th>
<th>A&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Output (Write) cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Data bus to Port A</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Data bus to Port B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Data bus to Port C</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Data bus to CWR</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RD</th>
<th>WR</th>
<th>CS</th>
<th>A&lt;sub&gt;1&lt;/sub&gt;</th>
<th>A&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Data bus tristated</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Data bus tristated</td>
</tr>
</tbody>
</table>

**Control Word Register**
Ports & Modes in 8255

- **Port A**
  - Mode 0: Simple I/O for Ports A, B & C
  - Mode 1: HS mode for Ports A and/or B
  - Mode 2: Bidirectional Data mode for Port A
    - B can in mode 0/1
    - Port C bits are used for HS

- **Port B**

- **Port C**
  - BSR Mode: Bit Set/Reset
    - For Port C
    - No Effect on I/O Mode
Basic Mode Definitions and Bus Int

- **Mode 0**
  - Basic I/O
- **Mode 1**
  - Strobe I/O
- **Mode 2**
  - Bi-Dir Bus
The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions.

Modes may be combined so that their functional definition can be suited to almost any I/O structure.

For instance:
- Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results,
- Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.
CONTROL WORD: control word format for I/O mode is shown in fig below. It is essential to understand this format.

- In interfacing applications
  - we have to determine the control word for programming the ports for input or output and write it into the CONTROL REGISTER before the data transfer program
  - This way of determining and writing the CONTROL WORD is called I/O programming.
Control Word Format for I/O Mode

D7 D6 D5 D4 D3 D2 D1 D0

Group B
- PORT CL (PC3-PC0)
  1 = INPUT; 0 = OUTPUT
- PORT B
  1 = INPUT; 0 = OUTPUT
- MODE SELECTION
  0 = MODE0; 1 = MODE 1

Group A
- PORT Cu (PC7-PC4)
  1 = INPUT; 0 = OUTPUT
- PORT A
  1 = INPUT; 0 = OUTPUT
- MODE SELECTION
  00 = MODE 0; 01 = MODE 1; 1X = MODE 2

1 = I/O Mode
0 = BSR Mode
To communicate with peripherals through 8255A, three steps are necessary:

- Determine the addresses of ports & control register from the chip select logic.
- Write a control word into the control register.
- Write instructions to transfer data to the peripherals through ports A, B & C.
Mode 0: Simple Input or Output

- Ports A, B & C are programmed for simple I/O.
- Data can be simply read from and written to the input and output ports respectively, after appropriate initialization.
- Outputs are latched.
- Inputs are not latched.
- Ports do not have handshake or interrupt capability.
- It is used when timing characteristics of I/O devices is well known.
Mode 0 Port Definition

<table>
<thead>
<tr>
<th>A (D4, D3, D1, D0)</th>
<th>B (D0, D1)</th>
<th>GROUP A</th>
<th>PORT C (Upper)</th>
<th>GROUP B</th>
<th>PORT B</th>
<th>PORT C (Lower)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>00</td>
<td>Output</td>
<td>Output</td>
<td>0</td>
<td>Output</td>
<td>Output</td>
</tr>
<tr>
<td>0001</td>
<td>00</td>
<td>Output</td>
<td>Output</td>
<td>1</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>0010</td>
<td>01</td>
<td>Output</td>
<td>Output</td>
<td>2</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>0011</td>
<td>01</td>
<td>Output</td>
<td>Output</td>
<td>3</td>
<td>Input</td>
<td>Input</td>
</tr>
<tr>
<td>0100</td>
<td>00</td>
<td>Output</td>
<td>Input</td>
<td>4</td>
<td>Output</td>
<td>Output</td>
</tr>
<tr>
<td>0101</td>
<td>01</td>
<td>Output</td>
<td>Input</td>
<td>5</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>0110</td>
<td>10</td>
<td>Output</td>
<td>Input</td>
<td>6</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>0111</td>
<td>11</td>
<td>Output</td>
<td>Input</td>
<td>7</td>
<td>Input</td>
<td>Input</td>
</tr>
<tr>
<td>1000</td>
<td>00</td>
<td>Input</td>
<td>Output</td>
<td>8</td>
<td>Output</td>
<td>Output</td>
</tr>
<tr>
<td>1001</td>
<td>01</td>
<td>Input</td>
<td>Output</td>
<td>9</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>1010</td>
<td>10</td>
<td>Input</td>
<td>Output</td>
<td>10</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>1011</td>
<td>11</td>
<td>Input</td>
<td>Output</td>
<td>11</td>
<td>Input</td>
<td>Input</td>
</tr>
<tr>
<td>1100</td>
<td>00</td>
<td>Input</td>
<td>Input</td>
<td>12</td>
<td>Output</td>
<td>Output</td>
</tr>
<tr>
<td>1101</td>
<td>01</td>
<td>Input</td>
<td>Input</td>
<td>13</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>1110</td>
<td>10</td>
<td>Input</td>
<td>Input</td>
<td>14</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>1111</td>
<td>11</td>
<td>Input</td>
<td>Input</td>
<td>15</td>
<td>Input</td>
<td>Input</td>
</tr>
</tbody>
</table>
Contd.

CONTROL WORD #0

```
D7  D6  D5  D4  D3  D2  D1  D0
1   0   0   0   0   0   0   0
```

CONTROL WORD #1

```
D7  D6  D5  D4  D3  D2  D1  D0
1   0   0   0   0   0   0   1
```

---

92C55A

A

B

8

PA7 - PA0

PC7 - PC4

PC3 - PC0

PB7 - PB0
Contd.

**CONTROL WORD #2**

```
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 1 0
```

```
82C55A

D7 - D0

PA7 - PA0
PC7 - PC4
PC3 - PC0
PB7 - PB0
```

**CONTROL WORD #3**

```
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 1 1
```

```
82C55A

D7 - D0

PA7 - PA0
PC7 - PC4
PC3 - PC0
PB7 - PB0
```
Contd.

**CONTROL WORD #4**

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

82C55A

- A
- C

- D7 - D0
- PA7 - PA0
- PC7 - PC4
- PC3 - PC0
- PB7 - PB0

**CONTROL WORD #5**

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

82C55A

- A
- C

- D7 - D0
- PA7 - PA0
- PC7 - PC4
- PC3 - PC0
- PB7 - PB0
Control Word #6

D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 1 0 1 0

82C55A

A

8
PA7 - PA0

4
PC7 - PC4

4
PC3 - PC0

B

8
PB7 - PB0

D7 - D0

Control Word #7

D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 1 0 1 1

82C55A

A

8
PA7 - PA0

4
PC7 - PC4

4
PC3 - PC0

B

8
PB7 - PB0

D7 - D0
Contd.

CONTROL WORD #8

D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1 0 0 0 0

82C55A

D7 - D0

A

8 PA7 - PA0

PC7 - PC4

PC3 - PC0

PB7 - PB0

CONTROL WORD #9

D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1 0 0 0 1

82C55A

D7 - D0

A

8 PA7 - PA0

PC7 - PC4

PC3 - PC0

PB7 - PB0
Contd.

**CONTROL WORD #10**

```
D7  D6  D5  D4  D3  D2  D1  D0
10010010
```

![Diagram of 82C55A with connections]

**CONTROL WORD #11**

```
D7  D6  D5  D4  D3  D2  D1  D0
10010011
```

![Diagram of 82C55A with connections]
Contd.
Contd.

CONTROL WORD #14

CONTROL WORD #15
Example

Write instructions to configure 8255 in the following ways. Assume port A address is A0H. All ports as input ports in mode 0.

Solution:

<table>
<thead>
<tr>
<th>Port</th>
<th>Address</th>
<th>Control Word</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA=A0H</td>
<td>A0H=1 0 1 0 0 0 0 0</td>
<td>PA=A0H=1 0 1 0 0 0 0 0</td>
<td>Control word: 1 0 0 1 1 0 1 1</td>
</tr>
<tr>
<td>PB=A1H</td>
<td>A1H=1 0 1 0 0 0 0 1</td>
<td>PB=A1H=1 0 1 0 0 0 0 1</td>
<td>9 BH</td>
</tr>
<tr>
<td>PC=A2H</td>
<td>A2H=1 0 1 0 0 0 1 0</td>
<td>PC=A2H=1 0 1 0 0 0 1 0</td>
<td>MVI A, 9BH</td>
</tr>
<tr>
<td>CR=A3H</td>
<td>A3H=1 0 1 0 0 0 1 1</td>
<td>CR=A3H=1 0 1 0 0 0 1 1</td>
<td>OUT A3H</td>
</tr>
</tbody>
</table>
Exercise

Write instructions to configure 8255 in the following ways. Assume port A address is A0H.

1. All ports as output ports in mode 0.
2. PA-O/P, PB-I/P, PCL and PCU-O/P in mode 0.
3. Configure Port A as input in Mode 0, Port B as output in mode 0, Port C (Lower) as output and Port C (Upper) as input ports.
Example: Twelve DIP switches are interfaced to 8255 via port B and port CL. Twelve LEDs are interfaced via port A and port CL as shown below.

Assume:

- All ports are in mode 0
- Identify the port addresses (PA, PB, PC, CW)
- Determine the control word to configure Ports.
- Write a program to read the DIP switches from port B and port CL and to display the readings at port A and port Cu respectively.
Fig: Interfacing 8255 I/O Ports in Mode 0
Contd.

- Identify the port addresses.
- Determine the control word to configure port A- & port Cu for output and port B and port C L for input.
- Write a program to read the DIP switches from port B and port C L and to display the readings at port A and port Cu respectively.
- From the circuit, observe that the control--signals MEMR and MEMW are connected.
- This indicates to us that the devices-are interfaced in MEMORY MAPPED MODE.
- So, they will have 16-bit addresses. CS is connected to A 15 through an inverter. So A 15 must be at logic high level for the 8255A to be selected.
The other 13 lines A14 - A2 are left without connection they can be considered as don't cares. Assuming these don't care lines to be at logic '0'. The addresses of the ports are:

<table>
<thead>
<tr>
<th>A15</th>
<th>A14 - A2</th>
<th>A1 A0</th>
<th>Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 ...... 0</td>
<td>0 0</td>
<td>Port A (8000) H</td>
</tr>
<tr>
<td>1</td>
<td>0 ...... 0</td>
<td>0 1</td>
<td>Port B (8001) H</td>
</tr>
<tr>
<td>1</td>
<td>0 ...... 0</td>
<td>1 0</td>
<td>Port C (8002) H</td>
</tr>
<tr>
<td>1</td>
<td>0 ...... 0</td>
<td>1 1</td>
<td>Control Reg (8003) H</td>
</tr>
</tbody>
</table>

To determine the control word we know that:

D7 = 1 for I/O mode;

D6, D5 = 0, 0 for mode 0 group A

D4 = 0 port A for output

D3 = 0 port Cu for output

D2 = 0 for mode 0 group B

D1 = 1 port B for input

D0 = 1 port CL for input.

Putting these bit values, we get the control word as:

D7 D6 D5 D4 D3 D2 D1 D0  
1 0 0 0 0 0 1 1  

=> (83)H.
Contd.

- Program for reading the switches and displaying LED Ports:

  MVI A, 83H
  STA 8003H ; Write control, word to initialize ports..
  LDA 8001H ; Read switches from port B
  STA 8000H ; Display at port A;
  LDA 8002 ; Read-switches from port C
  ANI OFH ; Mask the four most significant bits; 4
  RLC ; Bring the 4 least significant bits into
  RLC ; upper half of the accumulator;
  RLC
  RLC
  STA 8002H ; Display them at port Cu.
  HLT
Mode 1 – Input/output with Handshake

- In mode 0, which is used for simple I/O, it is assumed that the peripheral devices are always ready.
- The microprocessor, therefore, need not to check their status before transferring data to and from.
- However this is not the case always.
  - Sometimes in order to check the-status, the Mp and the peripherals exchange a few signals prior to actual data transfer.
  - These signals are called hand shake signals.
  - The 8255A's capability to transfer data with handshake is provided in its mode 1 operation.
Contd...

- **Feature of Mode 1:**
  - This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “handshaking” signals.
  - Port A and port B function as 8-bit I/O ports.
  - Each port uses three bits from port C as handshake signals. The remaining two bits from port C can be used for simple I/O.
  - Input-data and output data are latched.
  - Used when timing characteristics of I/O devices is not well known, or used when I/O devices supply or receive data at irregular intervals.
When port A and port B are configured as input ports, they use three bits each from port C as handshake signals.

Port A uses PC3, PC4 and PC5 bits and port B uses PC0, PC1 and PC2 bits.

These are shown in figure. These control signals are named STB, IBF and INTR. The purpose, of these signals is as follows.
Contd.

Fig: Mode 1 Input Configuration
Contd. Mode 1 input Control Signals

STB (Strobe Input): This is an active low signal, generated by the input device, when a byte of data is transmitted.

- On receipt of this signal, the 8255 generates two signals, IBF and INTR.

- IBF is routed to the input device and INTR to the microprocessor.

- IBF (Input Buffer Full): This is an active high signal. It tells the peripheral device that the previous byte sent by the device is there in the buffer and the microprocessor is yet to read the same. This kind of acknowledgement and information enables the peripheral to defer sending the next data byte until the buffer is empty, which is indicated by IBF going low.

- The IBF signal is deactivated when CPU reads the data from input buffer of the respective port by activation of RD signal.
**CONT'D. MODE 1 INPUT CONTROL SIGNALS**

- **INTR** (Interrupt Request): This is an output signal generated by 8255 in response to IBF, STB and INTE (Interrupt enable).

- This is used to interrupt the microprocessor to read the data byte from the buffer.

- **INTE**: It is an internal flip-flop for enabling or disabling INTR signal.

- The two flip-flops INTEA and INTEB are set/reset by using the BSR mode.
MODE 1 Control word: To configure port A and port B as input ports, the mode 1 control word is as follows.
MODE 1 Status word: The status word is constituted by port C bits. When the microprocessor reads port C, the status word is placed in accumulator.

Then the microprocessor can examine the bits to determine the status. The status word is shown below.
When port A and/or port B are configured as output ports, both of them use bits from port C as handshake signals. These handshake signals are as follows, and are shown in below.

Fig : Mode 1 Output Configuration
Contd. Mode 1 Output Control Signals

- **OBF: (Output Buffer Full)** - This is an active low signal generated by 8255A to indicate to the peripheral that the microprocessor has written one byte of data into the output port and that it is ready to be read by the device from the port.

- **ACK: (Acknowledge):** This is an input signal from the peripheral to 8255, indicating that it has received the byte from the port.
  - It is active low.
Contd. Mode 1 Output Control Signals

- **INTR: (Interrupt Request)** - This is an output signal generated by 8255.
  - It is set by OBF, ACK and INTE.
  - It can be used to interrupt the MPU for the next data byte.

- **INTE: (Interrupt Enable)**: This is an internal flip-flop to enable interrupts.
  - The two flip-flops INTEA and INTEB are controlled by the bits PC6 and PC2 respectively through BSR mode.

- **PC4, PC5**: These two lines can be setup either as input or output.
Contd. Mode 1 Output Control Signals

- MODE 1 Control word: To configure port A and port B as Output ports, the mode 1 control word is as follows.

![Diagram showing Mode 1 control word and port configurations.](image)
Contd. Mode 1 Output Control Signals

- **MODE 1 Status word**: The status word is accessed by issuing a read to port C.

- To configure port A and port B as Output ports, the mode 1 control word is as follows.

```

D_7  D_6  D_5  D_4  D_3  D_2  D_1  D_0

OBF_A  INTE_A  I/O  I/O  INTRA_A  INTE_B  OBF_B  INTER_B

GROUP A    GROUP B

```
Exercise

Write instructions to configure 8255 in the following ways. Assume port A address is A0H.

1. PA-I/P, PB-O/P in mode 1
2. Configure Port A as input in Mode 1, Port B as output in mode 1, Port C7-6 as input ports.
Mode 2 – Strobed Bidirectional Bus I/O

- This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O).
- “Handshaking” signals are provided to maintain proper bus flow discipline in a similar manner to MODE.
- It is used with an I/O device that receives data some times and sends data sometimes.
- Ex. Hard disk drive.
- Mode 2 operation is useful when timing characteristics of I/O devices is not well known, or when I/O devices supply or receive data at irregular intervals.
Contd. Mode 2 – Strobed Bidirectional Bus I/O

- Port A can be configured as the bidirectional port and Port B either in mode 0 or mode 1.
- Port A uses five signals from Port C as handshake signals for data transfer.
- The remaining three lines from Port C can be used either as simple I/O or as handshake signals for Port B.
- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both Inputs and Outputs are latched.
Exercise

Write instructions to configure 8255 in the following ways. Assume port A address is A0H.

1. PA-Bidirectional port, PB-I/P in mode 1
2. Configure Port A in Mode 2, Port B as output in mode 1. (PC7-3 are handshake lines for Port A and PC2-0 are handshake signals for port B).
Bit Set/Reset, Control word and control register

- Any of the eight bits of Port C can be Set or Reset using a single Output instruction.
- In this mode, individual bits of port C can be used for applications such as on Off switch.
- BSR control word has D7 = 0;
- When Port C is being used as status/control for Port A or B these Bits can be set or reset by using the Bit set/reset operation just as if they were data output port.
- This feature reduces software requirements in Control-based applications
Contd.

**Fig: BSR Control Word Format in the BSR Mode**
Exercise

Write instructions to configure 8255 in the following ways. Assume port A address is A0H.

1. Set to 1 bit 4 of Port C

\[ \begin{array}{cccccccc}
0 & x & x & x & 1 & 0 & 0 & 1 \\
\end{array} \]

\[ \text{09H} \]
\[ \text{Mvi A, 09H} \]
\[ \text{out A3H} \]

Exercise

1. Reset to 0 bit 6 of Port C
Exercise

1. Write instructions to configure 8255 in the following ways. To set PC4 and PC6 pins of port C for 5 mse and reset it after that.

Assume:
- port A address is B0H. And
- delay routine is available.

2. Write a program to blink Port C bit 0 of the 8255 infinitely. Assume address of control word register of 8255 is 83H.

Assume: Delay routine is available.
- 8086 microprocessor
1. Consider the interface circuit shown in fig (a) below and write a BSR control word subroutine to set PC7 and PC3 and reset them after 10 ms.

- Assume that delay routine is available.